IN THE PCT

BEFORE THE INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

IN RE APPLICATION

International Application No.	PCT/CA2003/001278
International Filing Date:	21 August 2003 (21.08.2003)
Priority Date:	29 August 2002 (29.08.2002)
Int'l Patent Classification No.	H01L31/0224
Applicant:	DAY4 ENERGY INC. et al
Title:	ELECTRODE FOR PHOTOVOLTAIC CELLS, PHOTOVOLTAIC CELL AND PHOTOVOLTAIC MODULE
Examiner:	A. Werner
Formalities Officer:	R. Andreatta
Agent's Reference:	49709-1
Reply Due:	**15 July 2004 (15.07.2004)**

June 22, 2004

European Patent Office
D-80298 Munich
GERMANY

BY COURIER

Attention: International Preliminary Examining Authority

Dear Sirs:

REPLY TO WRITTEN OPINION MAILED 15.04.2004

Amendments

There are no amendments to the application at this time.

Composition of Application after the above amendments

The arguments and comments submitted herein relate to the application composed as follows:

Description: Pages 3-14 as originally filed;
Pages 1, 2, 2a as per the amendment filed March 12, 2004;

Response to item V: Re: Article 33, Novelty, Inventive Step, etc.

The Examiner states that the subject matter of claims 1-19 does not involve an inventive step (Art. 33(3)) in view of D1:US 4 380 112 (Little) and D2:EP-A-0 807 980 (Canon KK).

Applicant's claim 1 recites an electrode comprising an electrically insulating optically transparent film, a surface of which carries an adhesive layer in which wires are embedded such that a surface of the wires protrudes from the adhesive. This protruding surface is covered with a coating comprised of an alloy with a low melting point for connecting the wires to a terminal bar and to an exposed junction side surface of a wafer.

D1 fails to disclose or suggest the use of a transparent film, rather, it discloses the use of a plate, preferably square, formed of glass such as Corning type 7070 or an organic glass.

D1 also fails to disclose or suggest the use of an adhesive layer on the transparent film, in which the wires are embedded such that a protruding surface of the wires with a low melting point alloy is exposed to the side surface of the PV element and connected thereto by melting the alloy. Rather D1 describes forming an antireflective coating on an inner surface of the glass plate and heating and pressing the wires into the plate, causing the plate to deform about the wires and the conductive buses to produce a coplanar metal-glass surface. Applicant's invention avoids the need to heat the wire carrying medium (the transparent film) to a high temperature, e.g. 700 degrees Celsius, and avoids the need to press with a pressure of 200 psi suggested in the example provided in D1 in column 12 at line 57, to deform the wire carrying medium to hold the wires in position for application to the exposed junction side surface of the semiconductor wafer.

Since the desired result of the process for securing the wires and bus bars to the cover plate described in D1 is a cover plate with a coplanar surface, there is no disclosure or suggestion that this surface should be non-coplanar such that surfaces of the wires should protrude from an adhesive layer on a transparent film, as claimed by the present applicant. The protruding surface claimed by the present applicant, with the low melting point alloy on it, facilitates application of the wires on the exposed junction surfaces of the wafer along their total length and securing by means of soldering.

As noted by the Examiner D1 fails to provide any disclosure or suggestion to employ a low melting point alloy to electrically connect the wires to the exposed junction surface of the wafer. Rather, D1 describes the use of electrostatic bonding to bond the cover plate inner surface 32, with the mesh and bus components embedded therein to the exposed junction side surface 52 of the previously processed semiconductor wafer 50. D1 states that Electrostatic

bonding involves heating the glass to a temperature at which ionic conduction within the glass can take place, followed by applying a strong electric field across the glass and material to be sealed. This would appear to require that the surfaces to be electrostatically bonded be smooth and coplanar, which would prohibit applicant's claim limitation that the surfaces of the wires protrude from the adhesive layer since this is not a coplanar surface.

Applicant's invention avoids the need for the complex process of electrostatic bonding described by D1. There is nothing in D1 or in the combination of D1 and D2 to suggest that this process of electrostatic bonding should be replaced with a method involving a low melting point alloy, nor is there anything to suggest that in order to employ a low melting point alloy, it would be desirable to permit a portion of the wires to protrude from an adhesive coating on a transparent film, or that the same method used to connect the wires to the exposed wafer surface, i.e. a low melting point alloy, can or should be used to electrically connect the wires to a terminal bar. There is clearly nothing that would lead one of ordinary skill in the art directly and without difficulty to the applicant's invention. Consequently, the applicant's claims are not obvious and satisfy the requirements under Article 33(3).

The remaining claims ultimately rely on the structure recited in claim 1 and therefore these claims should also comply with PCT Article 33(3) due to the additional subject matter they recite and due to their ultimate dependence upon claim 1 which has been shown above to comply with PCT Article 33(3).

Applicant respectfully requests that a favourable International Preliminary Examination Report be issued for this application.

John W. Knox
FETHERSTONHAUGH & CO.
Box 11560 Vancouver Centre
Suite 2200, 650 West Georgia Street
Vancouver, British Columbia
Canada V6B 4N8

JWK:cmm